REMARKS

All rejections and objections set forth in the Office Action mailed April 27, 2011 (hereinafter "the Office Action") are respectfully traversed.

Claims 1-60 were examined. By this amendment, Applicant is amending the title; canceling claims 1, 3, 15, 17-20, 26, 29, 31-35, 38, 41, 43, 45, 48, 52 and 55; and amending claims 2, 4, 7 - 14, 16, 21, 30, 36, 37, 39, 40, 42, 44, 49, 53, 56 and 58. Applicant respectfully submits that no new matter has been added as support for the amendments to the claims is found in the original specification at least at page 15, line 1 - page 16, line 9.

In the Specification

The title of the invention was objected to as not being descriptive. The Office Action suggested an amendment to the title that the Applicant has adopted. Accordingly, Applicant requests that the objection to the title be withdrawn.

Claim Objections

Claims 7, 15, 29 and 35 were objected to due to informalities set forth in the Office Action. Applicant has amended claim 7 to remove the extraneous semicolon and claims 15, 29 and 35 have been canceled. Applicant believes the objection has been overcome.

Rejections Under 35 USC §112

Claims 21-24 and 31-34 stand rejected for being "single means" claims. Claims 31-34 have been canceled and independent claim 21, from which claims 22-24 depend, has been amended such that it is no longer a "single means" claim. Accordingly, Applicant submits that claims 21-24 comply with §112.

Claims 13, 16, 38, 39 and 41-45 stand rejected for reciting "means for" in a method claim. Claims 13 and 16 have been amended to remove the "means for" language, claims 38, 41, 43 and 45 have been canceled, and claim 39 has been amended to depend on claim 37 (previously dependent on claim 38). Applicant submits that the claims have been clarified and the objection can be withdrawn.

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Rejections Under 35 USC §102

Claims 1-12, 14, 15, 17-25, 27-29, 31-37, 40, 46, 47 and 51 stand rejected as being anticipated by Ussery, U.S.P. 6,484,304. Applicant respectfully traverses.

Applicant has canceled claims 1, 3, 15, 17-20, 29, 31-35. Independent claim 2 has been amended to incorporate subject matter from claim 4, specifically related to the "means for identifying bit demands." Independent claim 8 has been amended to incorporate subject matter from claim 13 regarding "identifying bit demands." Independent claim 21 has been amended to incorporate subject matter from claim 26 regarding "means for identifying bit demands."

Applicant respectfully submits that the rejections of these claims under §102 has been rendered moot by these amendments to the claims. Applicant will address the rejections of the claims below in response to the §103 rejections set forth in the Office Action.

Rejections Under 35 USC §103

Claims 13, 15, 26 30, 38, 39, 41-45, 48-50 and 52-60 stand rejected under §103 as being unpatentable over Ussery in view of Shackleford, U.S.P. 5,896,521. Applicant respectfully traverses.

Ussery is directed to a method for generating an application specific integrated circuit (ASIC) that includes a software configurable semiconductor integrated circuit having a fixed hardware architecture that includes a plurality of task engines. (Abstract) Ussery discloses that application libraries are generated that define component objects that are used as building blocks in developing an application for a programmable system architecture (PSA) integrated circuit. (Col. 4, lines 23-48). The use of application libraries reduces the design cycle time and the level of skill required to produce the integrated circuit. (Col. 4, lines 56-58).

Independent claim 2, as amended, recites:

> An application specific coprocessor system for use with a processor for use in massive data manipulations specific to an application and adapted for attachment to a workstation having a general purpose processor, said coprocessor system having programming code which is assembled as instructions for said specific application in

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> combination with accelerator environment specific requirements, independently provided, wherein
>
> said environment specific instructions are accessed by a compiler in response to user input in an application specific form; and
>
> wherein said compiler comprises:
>
> a user interface to permit an application trained non circuit design trained user to enter instructions to achieve application specific accelerated processing;
>
> means for creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs; and
>
> means for identifying bit demands for the application specific accelerated processing needs such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives. (emphasis added)

The Office Action acknowledges that Ussery does not disclose "means for identifying bit demands" but points to Shackleford for remedying this deficiency. Applicant respectfully submits that the combination of Ussery and Shackleford does not render obvious that which is recited in claim 2, as amended.

Shackleford is directed to a processor synthesis system and a processor synthesis method for implementing an ASIC. (Col. 3, lines 6-8). Shackleford is directed to the problem of placing a CPU in an ASIC where the CPU is predefined with a bit width that may be more than is necessary. Using a larger than necessary CPU in an ASIC takes up additional room in the device. A CPU is synthesized that does not depend on a specific process technology and has the bit width customized to the requirements of the specific application. (Col. 3, lines 43-46). More specifically, the CPU bit width is customized, "for example, when an 11-bit processor is required for a predetermined application, an 11-bit processor is synthesized instead of a 16-bit or 32-bit processor." (Col. 6, lines 50-57).

The cited combination, however, does not result in an application specific coprocessor system with a compiler that comprises "means for identifying bit demands…such that each intermediate step in a calculation is allocated a minimal number of bits necessary" for producing a

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"final result that fulfills domain-specific objectives," as recited in claim 2, as amended. Applicant respectfully submits that Shackleford's teaching of customizing the CPU to the smallest bit width, in order to take up the least space in an ASIC, is not the same as allocating "a minimal number of bits necessary" for each "intermediate step," as recited above.

For at least the foregoing reason, Applicant respectfully submits that independent claim 2, and its dependent claims, are allowable over the cited combination of references.

Independent claim 8, as amended, recites:

> A method for programming an accelerating coprocessor comprising the steps of:
> accessing data reflective of programming requirements for a general area of applications; and
> identifying bit demands for the accelerating coprocessor acceleration function such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives. (emphasis added).

Applicant respectfully submits that independent claim 8, and its dependent claims, are patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

Independent claim 16, as amended, recites:

> A method of compiling data for programming an accelerating coprocessor comprising the steps of:
> creating an internal representation reflecting the operational characteristics of the coprocessor corresponding to application specific accelerated processing needs; and
> identifying bit demands for the application specific accelerated processing needs such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives. (emphasis added).

Applicant respectfully submits that independent claim 16 is patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

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Independent claim 21, as amended), recites:

> A compiler for programming an accelerating coprocessor comprising:
>
> means for accessing data reflective of programming requirements for a general area of applications; and
>
> means for identifying bit demands for the accelerating coprocessor such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives. (emphasis added).

Applicant respectfully submits that independent claim 21, and its dependent claims, are patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

Independent claim 30, as amended, recites:

> A compiler for data for programming an accelerating coprocessor comprising:
>
> means for creating an internal representation reflecting the operational characteristics of the accelerating coprocessor corresponding to application specific accelerated processing needs; and
>
> means for identifying bit demands for the application specific accelerated processing such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives. (emphasis added).

Applicant respectfully submits that independent claim 30 is patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

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In view of the foregoing, Applicant believes the pending claims are in condition for allowance and a notice to this effect is earnestly solicited. The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application. The Examiner is hereby authorized to charge any fees due to this submission, or credit any balance, to Deposit Account No. 23-0804.

Respectfully submitted,

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